AMENDMENTS TO THE CLAIMS

A detailed listing of all claims that are, or were, in the present application, irrespective of whether the claim(s) remains under examination in the application are presented below. The claims are presented in ascending order and each includes one status identifier. Those claims not cancelled or withdrawn but amended by the current amendment utilize the following notations for amendment: 1. deleted matter is shown by strikethrough for six or more characters and double brackets for five or less characters; and 2. added matter is shown by underlining.

1-12. (Canceled)

13. (Currently Amended) A memory unit comprising:

a memory having a main memory area and a spare memory area, wherein said main memory area includes a plurality of data storage registers and wherein each of said data storage registers has an address, and wherein said spare memory area has a storage capacity;

a display; and

a processor, wherein said processor transfers data stored in each of said addresses of said main memory area to said spare memory area upon a number of write operations performed to a respective one of said addresses in said main memory reaching a predetermined value, and wherein said processor drives said display upon said number of write operations performed to a respective one of said addresses in said main memory reaching a predetermined number ~~to display a remaining amount of said storage capacity~~

~~in said spare memory upon a remaining amount of said storage capacity reaching a predetermined remaining capacity~~.

14. (Currently Amended) The memory unit as in claim 13, wherein said processor compares said number of write operation performed with a plurality of different values of said predetermined values ~~remaining amount of said storage capacity with a plurality of different values of said predetermined remaining capacity~~, wherein the comparison produces a plurality of different results, and wherein said processor drives said display in different manners dependent upon said plurality of different results.

15. (Cancelled)

16. (Currently Amended) A memory unit comprising:

a memory having a main memory area and a spare memory area, wherein said main memory area includes a plurality of data storage registers and wherein each of said data storage registers has an address, and wherein said spare memory area has a storage capacity;

a display; and

a processor, wherein said processor transfers data stored in each of said addresses of said main memory area to said spare memory area upon an error frequency within one of said plurality of data storage registers reaching a predetermined frequency, and wherein said processor drives said display upon said error frequency reaching a predetermined frequency ~~to display a remaining amount of said storage capacity in said~~

~~spare memory upon a remaining amount of said storage capacity reaching a predetermined remaining capacity~~.

17. (Currently Amended) The memory unit of claim 16, wherein said processor compares said error frequency with a plurality of different values of said predetermined values ~~remaining amount of said storage capacity with a plurality of different values of said predetermined remaining capacity~~, wherein the comparison produces a plurality of different results, and wherein said processor drives said display in different manners dependent upon said plurality of different results.

18 - 24. (Cancelled)

[Please add new claims 25-33:]

25. (New) A memory unit comprising:

a flash memory having a main memory area and a spare memory area, wherein said main memory area includes a plurality of data storage registers and wherein each of said data storage registers has an address, and wherein said spare memory area has a storage capacity;

a display; and

a processor wherein said processor transfers data stored in each of said addresses of said main memory area to said spare memory area upon a number of write operations performed to a respective one of said addresses in said main memory reaching a

predetermined value, and wherein said processor drives said display to display a normal status when the number of write operations has not reached a first set value, a warning status when the number of write operations has reached the first set value but not a second set value, and an extreme limit status when the number of write operations has reached a second set value.

26. (New) The memory unit as in claim 25, wherein a remaining amount of the storage capacity in said spare memory does not reach a first set remaining amount in the normal status, and the remaining amount of the storage capacity reaches the first set remaining amount but does not exceed the second set remaining amount in the warning status, and the remaining amount of the storage capacity exceeds a second set remaining amount in the extreme limit status, and the display is driven to display the normal status, the warning status and the extreme limit status in a distinguishable manner.

27. (New) The memory unit as in claim 25, wherein the normal status, the warning status and the extreme limit status are displayed in different manners.

28. (New) The memory unit as in claim 27, wherein the normal status, the warning status and the extreme limit status are displayed by using different colors.

29. (New) The memory unit as in claim 28, wherein the normal status, the warning status and the extreme limit status are displayed by using blue, yellow and red, respectively.

30. (New) The memory unit as in claim 26, wherein the normal status, the warning status and the extreme limit status are displayed in different manners.

31. (New) The memory unit as in claim 30, wherein the normal status, the warning status and the extreme limit status are displayed by using different colors.

32. (New) The memory unit as in claim 31, wherein the normal status, the warning status and the extreme limit status are displayed by using blue, yellow and red, respectively.

33. (New) A flash memory unit comprising:

a flash memory area, wherein said flash memory area stores data and wherein said flash memory area has a limited useful life in storing said data;

a spare memory area having a data storage capacity;

a display; and

a processor, wherein said processor transfers the stored data of said flash memory area to said spare memory area upon said flash memory approaching said limited useful life, and wherein said processor drives said display to display an amount of remaining data storage capacity in said spare memory, wherein the status of the display provides an indication as to whether replacement of said flash memory area is required..

34. (New) The flash memory unit of claim 33 wherein the limited useful life is indicated by an increase in error frequency or by a finite number of read/write operations.